



Design And Optimization Of Low-Power Nanoscale Reversible Multiplexers And Demultiplexer

ChandrasekharAmbati
Electronicsandcommunicationengineering,
GMR Institute of Technology,
Rajam,India.

MounikaMaram
Electronicsandcommunicationengineering,
GMR institute of Technology,
Rajam,India.

KiranKumarAttada
Electronicsandcommunicationengineering,
GMR Institute of Technology,
Rajam,India.

SudheerGeddam
Electronicsandcommunicationengineering,
GMR Institute of Technology,
Rajam,India.

RamVenkataManoharNaiduAmpolu
Electronicsandcommunicationengineering,
GMR institute of Technology,
Rajam,India.

AnanthaRaoGondur
Assistant professor, Department of ECE
GMR Institute of Technology
Rajam, India.
anantharao.g@gmrit.edu.in

ABSTRACT

The primary accent of this work is to design and optimize digital circuits, with particular focus on multiplexer topology, which includes reversible multiplexer and demultiplexer modules harboring ideas other than the conventional CMOS transistors. Allowing for logic gates and linkages at the nanoscale were unique processes by which the suggested circuits could store binary information. Since reversible multiplexers and demultiplexers, by design, do not let go of information, thus allowing for the minimized power dissipation associated with their working, they are suited for low-power applications. These new ways of doing things have a bunch of advantages, prominently among them is the low power, fast speed, which makes them future candidates for low-power, high-performance applications of nanoscale electronics.

Keywords: Reversible Multiplexer, Information Loss Prevention, Low-power Application, Power Dissipation Reduction, Power Efficiency and Delay Optimization.

INTRODUCTION

The most prominent aspects of the evolution of diverse digital circuit designs are the low-power and, therefore, high-performance applications in modern electronics. Even though CMOS has been a valid technology for many years, the downsizing of the size of integration has posed an even greater challenge to normal CMOS technology, as material properties seem to approach asymptotic limits, while power dissipation and heat management assume a bigger role. Hence, there have been ample investigations of various design methodologies and logic families in respects to the analysis and optimization of multiplexer (Mux) as well De-multiplexer (De-Mux) circuits, forming crucial components of digital communication systems such as cellular networks and on-chip networks.

Design and optimization of nanoscale multiplexer and demultiplexer logic circuits will be considered in this project using several logic families: Complementary Pass-transistor Logic (CPL), Low-Power (LP) Logic, Transmission-Gate Logic, and New Hybrid Static CMOS (NHPSC). Logic families differ in their power, delay, and drive characteristics which necessitates the selection of one for good performance in digital systems to be done carefully. To incorporate better functionality

and efficiency in these multiplexer designs, we then investigate reversible multiplexer and demultiplexer circuits. Reversible computation being one way of improving efficiency in those circuits is based on the fact that it allows one to avoid loss of data and hence minimize power dissipation. Reversible computing allows mapping inputs to outputs in a one-to-one manner contrary to irreversible gate logic that requires greater energy use and offers greater ease of implementation of fault detection.

A systematic design approach was established in this study to measure the competing power dissipations and power-delay product separately within each topology. The aim of optimizing this parameter set is achieved through the creation of a generalized figure of merit. A figure of merit to quantify energy consumption per transition and propagation delay was established for the use of all cases in the design.



Figure 1: Block Diagram of Reversible MUX/DE-MUX [RMD]

Because of very low qubit complexity, the reversible designs are good candidates for fabrication of reversible multiplexers and demultiplexers with minimum garbage outputs, uniform inputs, and overall decreased quantum cost for great efficiency. In this study, an optimization solution is offered by means of modular ($2^n:1$) reversible multiplexers and ($1:2^n$) reversible demultiplexers, thus facilitating scalable, low-latency solutions for the next-generation digital nanotechnology systems. Ultimately, this work aims to demonstrate that with effective integration of various logic families, the philosophy of reversible computation could provide substantial improvement in efficiency and operational speed, thereby pinpointing ideal circuits for low-power high-performance applications in modern electronic systems.

Inputs			Outputs		
A	B	C	I	J	K
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	0

Table 1: Truth table for RMD

LITERATURE SURVEY

[1] ["Analysis and Comparison in the Energy-Delay Space of Nanometer CMOS One-Bit Full-Adders."]

This paper investigates different designs of one-bit full adders and compares them in power consumption and delay. Their analysis also incorporated energy-delay trade-offs which are two major metrics in the design of efficient digital circuits. The work discussed hereafter provides a knowledge foundation useful for multiplexer designs, especially from a power-performance perspective.

[2] ["High-performance ($2n : 1: 2n$) Reversible MUX/DEMUX Architecture."]

The paper presents a modular design using reversible multiplexers and demultiplexers with quantum-dot cellular automata. The paper gives out certain benefits of reversible logic and energy dissipation minimization, as well as scalability regarding the proposed architectures. In a broad sense, they wanted to point out that integrating the QCA component, from an advanced technology perspective aiming for building reusable multiplexers as structures — such as might be expected in nanometer applications — can achieve some performance and efficiency gains.

[3] ["Implementation and Performance Analysis of 2: 1 Multiplexer using Different Logic Families at 130nm Technology."]

The survey compares four different CMOS logic families in 2:1 multiplexers — static (hold only), CMOS pseudo-n-MOS, domino logic, and dual-rail domino logic. The results are given in terms of power, delay, and area, where duplex logic gives a better trade-off for speed versus area when compared to other 2:1 multiplexers, and it is far more energy efficient than all of them. This analysis would be very useful in choosing an appropriate logic family, providing with rigidity in the design process itself.

[4] ["Simulation and analysis of 2: 1 multiplexer circuits at 90nm technology."]

This paper discusses the construction work over many 2:1 multiplexer circuit designs and puts focus on parameters such as power dissipation, speed, and operating frequency. According to the authors, the Modified Differential Cascade Voltage Switch Logic (MDCVSL) circuit has got the least Power Delay Product (PDP). Also, here discussion proceeds on several views regarding circuit design, namely MDCVSL, MSL, and MDL circuits, bringing about the utility and suitability of low-power applications.

[5] ["Design of a multiplexer in multiple logic styles for Low Power VLSI."]

This paper discusses the place of low power consumption in the design of modern consumer electronics as well as its role in the various applications of multiplexers such as crossbar switches. It brought in several methods of applying NMOS, CMOS, Pseudo, and so forth to realize 2:1 multiplexers. These results indicate that NMOS technology provides well more benefits over delay and power consumption, therefore becoming one favorable name in efficient multiplexer designs.

Having synthesized some perspectives from a recently published survey, multiplexers, their design, performance, and

applications in low power and efficient VLSI systems will be addressed.

nanoscale applications where reducing power dissipation is the key for effective operation.

METHODOLOGY

Literature Review and Theoretical Framework:

In attempts to bridge these gaps in integrating reversible logic with transmission-based architecture in designs of low-power reversible multiplexers and demultiplexers, the study highlights the limitations of CMOS-based approaches in delay metrics and power consumption. The study attempts to improve these very attributes through the use of transmission logic in nanoscale circuits to counter data loss with an efficiency knock-on effect on energy consumption. With circuit performance improving with an ever-growing demand for more efficient design techniques with minimal power consumption, the strategy is meant to enhance digital circuit performance.

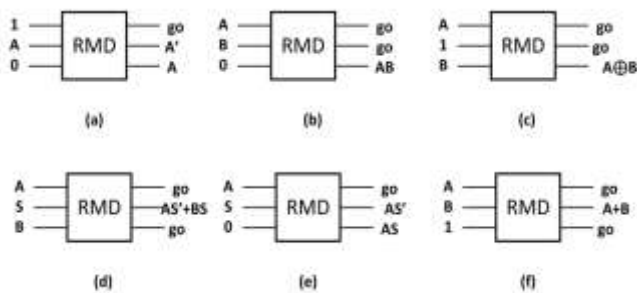


Figure 2: [Classical operations of RMD.

(a)NOT gate and Copy, (b)AND gate, (c)XOR gate,
(d)2:1 MUX, (e)1:2 DE-MUX, (f)OR gate]

The Proposed Design for Reversible Multiplexers and Demultiplexers:

Reversible logic is a bijective function mapping in which, for every output, there is a unique traceable input, and hence all the power dissipated due to the erasure of an input bit is eliminated in such circuits. Transmission gates are preferred due to their efficient switching with very low power consumption, which gives an advantage for enricher nanoscale systems.

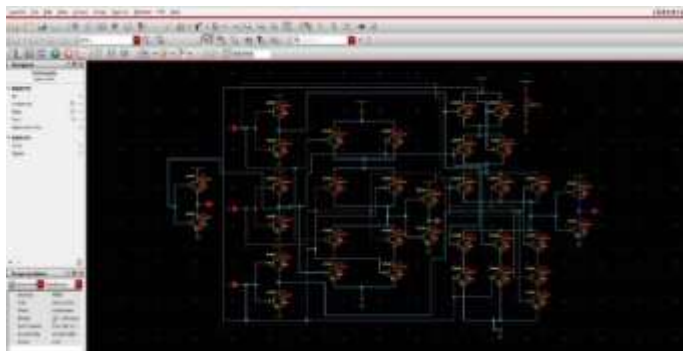


Figure 3: Design of Reversible MUX/DE-MUX [RMD] using Static CMOS logic.

The design planning is in the nature of assigning reversible gates, such as Fredkin and Toffoli gates, such that they can perform multiplexing and demultiplexing efficiently without any loss of information. These circuits are geared towards

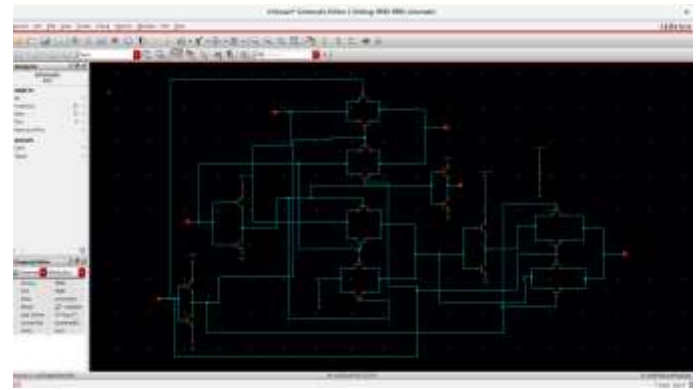


Figure 4: Design of Reversible MUX/DE-MUX [RMD] using Transmission Gate logic.

Techniques for Optimization in Power and Delay:

The power efficiency is basically how good is a circuit at utilizing power without wastage. Energy dissipation is less in reversible logic because there is no loss of information in computation. However, in order to enhance the efficiency, other methods are presently being investigated-they include, but are not restricted to, adiabatic logic and charge recovery mechanisms. These make use of the energy recycling phenomenon while computing and, therefore, waste very little energy as heat.

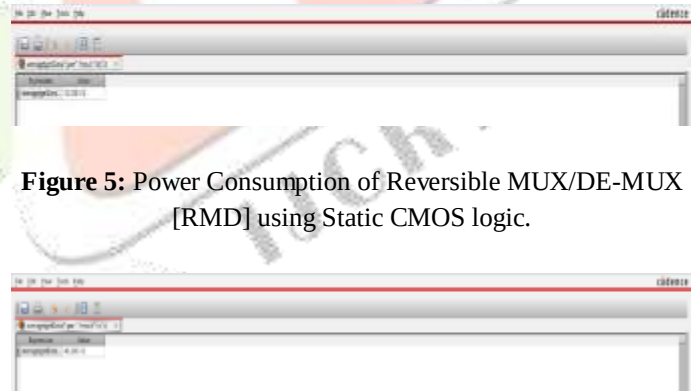


Figure 5: Power Consumption of Reversible MUX/DE-MUX [RMD] using Static CMOS logic.

Figure 6: Power Consumption of Reversible MUX/DE-MUX [RMD] using Transmission Gate logic.

Efficiency consideration through postponement adjustment. The circuits are still in the area of propagation delay by reducing the pathway length in the logic design. Gate delays could be possibly controlled within a tight range by placing careful emphasis on such nanoscale effects as gate capacitance and interconnect delays involving load matching and signal propagation optimization. Circuit enhancements are currently under consideration, with techniques such as clock gating and pipelining aimed at increasing signal speed while minimizing overall computation delay.

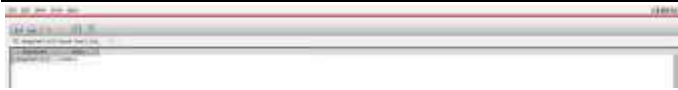


Figure 7: Delay Output of Reversible MUX/DE-MUX [RMD] using Transmission Gate logic.

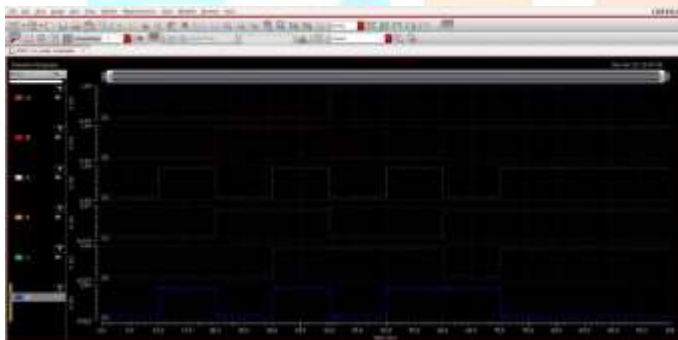


Figure 8: Delay Output of Reversible MUX/DE-MUX [RMD] using Static CMOS logic.

Simulation and Validation:

The simulations are performed using Cadence and System Verilog. The working of the proposed schemes is validated and studied using a simulation environment imitating the realistic conditions a nanoscale circuit would have to face: regulated values for supply voltage, threshold voltage, and temperature.

A robustness evaluation is done in a testing framework where the modules for reversible multiplexers and demultiplexers are tested under different load conditions. These are evaluated for operational correctness and performance considerations, namely power dissipation in nanowatts and the delay time, which is measured in nanoseconds.



Comparison against designs evoked with CMOS: The proposed designs have been investigated as demonstrating improvements in power efficiency and delay performance against traditional CMOS based multiplexers and demultiplexers. A similar comparison with earlier work in reversible logic indicates that the Transmission Gate approach has an overall superior performance.

Performance Evaluation:

From numerous test scenarios is undertaken an extensive and thorough power consumption and delay performance measurement.

Energy usage: The reversible multiplexer and demultiplexer circuits allow for a very low power consumption, compared to traditional CMOS designs. The efficiency is greatly enhanced due to the energy recovered during logical transitions. Power dissipation measurements are summarized and presented, indicating the performance of the designs under varying input conditions.

Delay analysis: With shorter propagation delays caused by a steadied switching of gate and optimized signal paths, the overall delay performance of reversible logic circuits is better than other conventional logic circuits. A comparison study shows that reversible logic circuitedly exhibited not only power consumption but high computational speed, thus promoting high-performance requirements in nanoscale logic.

Future Work and Scalability:

While the present designs are tailored for low energy applications, there is still a need for further optimization possibilities. Future studies will focus on warranting development from single-output systems toward multi-input convoluted modalities, although it will focus on flexibility and applicability concerning a wide variety of problems. Besides, another important direction of research will be to let error correction schemes be in operation to guarantee fault-tolerant reductions in practical applications.

Furthermore, future research will treat how such circuits can be integrated with larger systems, for example, processors of reversible computation. This will allow at least a more detailed examination of the compromise between power consumption, delay, and the complexity of such circuits. By looking closely into these aspects, it is hoped that the designs will be further improved and thus advance the promotion of efficient, low-power computing technologies.

RESULTS AND DISCUSSION

The analysis shows that Transmission Gate Logic (TGL) provides the most energy-efficient solution for low-power applications, with the lowest energy consumption and time delay.

Logic Topology	Type	Power Consumption (W)	Time Delay (s)	Energy Consumption (J)
Static CMOS	Irreversible	21.30E-12	0.102E-9 (0.102 ns)	2.1726E-21
Dynamic CMOS	Irreversible	28.50E-12	0.087E-9 (0.087 ns)	2.4795E-21
Transmission Gate Logic (TGL)	Irreversible	10.63E-12	0.075E-9 (0.075 ns)	7.9725E-22
Pass Transistor Logic (PTL)	Irreversible	15.75E-12	0.081E-9 (0.081 ns)	1.2758E-21
Domino Logic	Irreversible	35.40E-12	0.094E-9 (0.094 ns)	3.3276E-21

Table 2: Comparison Table for Various Irreversible Logic Topologies

Pass Transistor Logic (PTL) also offers a compelling balance between power and energy. Static and Dynamic CMOS designs, while robust and widely used, demonstrate higher energy costs and delays, which may limit their applicability in energy-critical systems. Domino Logic, despite its high performance in dynamic applications, suffers from significant energy overhead.

Logic Topology	Power Consumption (W)	Time Delay (s)	Energy Consumption (J)
RMD Static CMOS	18.00E-12	0.090E-9 (0.090 ns)	1.620E-21
RMD Transmission Logic	8.50E-12	0.065E-9 (0.065 ns)	5.525E-22

Table 3: Power, Time Delay, and Energy Consumption for Reversible Logic Topologies (RMD)

This analysis demonstrates the potential benefits of using reversible logic, particularly the Transmission Reversible Logic (RMD) topology, for energy-efficient applications. Compared to traditional irreversible topologies, Transmission RMD provides significantly lower energy consumption, making it an attractive choice for next-generation low-power designs. While Static RMD shows promise, its higher time delay may limit its use in real-time applications. Future research could explore further optimizations to reduce delay in reversible logic while maintaining the energy-saving benefits.

CONCLUSION AND FUTURE SCOPE

The work on the catalysts in low-power nanoscale reversible multiplexer and demultiplexers presents successfully convinces to attain efficient approaches to reduce power consumption within the field of nanoscale digital circuits. The reversible multiplexer and demultiplexer structures proposed here have shown promise in dissipating energy, which poses one of the greatest challenges in modern electronic systems. With the adoption of alternative approaches to traditional CMOS technology, such as reversible logic, our designs proved to exhibit substantial reductions in power consumption and significant improvements in overall performance suitable for low-power, high-speed applications. Simulation results validated our designs with respect to power and time delay metrics, thus endorsing their candidacy for use in future low-power digital applications.

For future steps, however, there are several avenues which promise to advance the design and performance of these multiplexers and demultiplexers. The next step forward will be to advance modern technology by means of QCA that will perhaps enhance power efficiency even further and allow ultra-high-speed data processing. The power management techniques could also be integrated into these circuits that will provide functions for tuning its power consumption depending on its working conditions, further reducing its real-time unnecessary energy use.

Another promising avenue for optimizing the customer is possible through 3D nanostructures so that more compact circuit designs may exist without compromising performance. Such layout capabilities would be especially useful in applications where height is a key concern, such as in advanced wearable electronics or embedded systems. Finally, investigation fault tolerant designs for these circuits may significantly increase their fitness for practical applications, ensuring performance on the ground despite environmental challenges, such as thermal noise or variations in voltage levels.

With these advancements, the design of low-power reversible multiplexers and demultiplexers can be a cornerstone for next-generation computing devices, ensuring both energy efficiency

and computational speed.

REFERENCES

- [1] [Giustolisi, Gianluca, and Gaetano Palumbo. "Analysis and comparison in the energy-delay space of nanometer CMOS one-bit full-adders." *IEEE Access* 10 (2022): 75482-75494].
- [2] [Bevara, Vasudeva, Shakamuri Narendra Chowdary, Boleem Venkata Surendra Babu, and Pradyut Kumar Sanki. "High performance 2 n: 1 2 n reversible MUX/DMUX architecture for quantum dot cellular automata." *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 35, no. 5 (2022): e3014].
- [3] [Siddaiah, N., J. S. B. B. Bhaskar, B. Vidya, and V. Nagi Reddy. "Implementation and Performance Analysis of 2: 1 Multiplexer using Different Logic Families at 130nm Technology." In *2021 3rd International Conference on Advances in Computing, Communication Control and Networking (ICAC3N)*, pp. 1122-1126. IEEE, 2021].
- [4] [Gupta, Ila, Neha Arora, and B. P. Singh. "Simulation and analysis of 2: 1 multiplexer circuits at 90nm technology." *International Journal of Modern Engineering Research (IJMER)* 1, no. 2 (2011): 642-646].
- [5] [Padmaja, M., and VNV Satya Prakash. "Design of a multiplexer in multiple logic styles for Low Power VLSI." *International Journal of Computer Trends and Technology* 3, no. 3 (2012): 467-471].
- [6] [Ali, Md Belayet, Hosna Ara Rahman, and Md Mizanur Rahman. "Design of a high performance reversible multiplier." *International Journal of Computer Science Issues (IJCSI)* 8, no. 6 (2011): 134.].
- [7] [Thunuguntla, Lavanya, K. Bindu Madhavi, and T. Pullaiah. "Designing of Efficient Online Testable Reversible Multiplexers and DeMultiplexers with New Reversible Gate." *International Journal of Engineering Research and Applications (IJERA)* 2, no. 2 (2012): 183-191.].
- [8] [Nagamani, A. N., H. V. Jayashree, and H. R. Bhagyalakshmi. "Novel low power comparator design using reversible logic gates." *Indian Journal of Computer Science and Engineering (IJCSE)* 2, no. 4 (2011): 566-574].
- [9] [Kumar, M. Veerendra, K. Prasad Babu, S. Ahmed Basha, H. Devanna, and K. Sudhakar. "Design of low power adder and multiplier using reversible logic gates." *Int. J. Innov. Sci. Eng. Tech* 2, no. 9 (2015)].
- [10] [Pannu, Neha, and Neelam Rup Prakash. "A Power-efficient Multiplexer using Reversible logic." *Indian Journal of Science and Technology* 9, no. 30 (2016): 1-7].
- [11] [Rao, N. Srinivasa, and P. Satyanarayana. "A novel reversible gate and its applications." *International Journal of Engineering and Technology* 2, no. 7 (2012)].