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An Intelligent Fuzzy Logic Control Strategy for a Single-Input Multi-Output DC–DC Converter in Electric Vehicle Applications

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Abstract— This paper extends a previously reported cross-regulation-free single-input three-output (SITO) DC-DC converter, originally regulated using classical Proportional-Integral (PI) controllers, by designing and implementing a Fuzzy Logic Controller (FLC) for each of its three independently controlled outputs — boost (V01), positive buck-boost (V02), and buck (V03). Unlike the linear PI controller, whose gains are fixed around a single operating point derived from small-signal averaged models, the proposed FLC uses the error and the change of error between the reference and the actual output voltage to nonlinearly adapt the duty-cycle correction, without requiring an explicit mathematical model of the converter. The open-loop, PI-controlled, and fuzzy-logic-controlled configurations of the converter are modeled and simulated in the MATLAB/Simulink environment under identical operating conditions, including input-voltage step disturbance and load step disturbance. Comparative simulation results show that the proposed FLC-based scheme achieves a faster dynamic response, reduced overshoot/undershoot, negligible steady-state error, and improved robustness to input voltage and load variation compared with the open-loop and PI-controlled systems, while preserving the inherent cross-regulation-free property of the converter topology. This study is restricted to MATLAB/Simulink-based simulation; no hardware prototype or experimental results are included.

Index Terms— Multiport converters, single-input multi-output (SIMO) converter, cross-regulation, fuzzy logic controller (FLC), PI controller, electric vehicle (EV), MATLAB/Simulink.

INTRODUCTION

Multiport DC-DC converters play an important role in electric vehicle (EV) auxiliary power supply systems, portable electronics, and hybrid renewable-energy interfaces, since a single-input multi-output (SIMO) structure can generate several independently regulated output voltages while reducing component count, size, and cost compared with multiple discrete single-input single-output converters [1]–[7]. A major challenge in conventional single-inductor SIMO converters is the cross-regulation problem, in which a change in the load current of one output disturbs the voltage of the other outputs, because the energy stored in the shared inductor is distributed among all the outputs [8]–[14].

A cross-regulation-free single-input three-output (SITO) converter was recently proposed, in which each output — boost (V01), positive buck-boost (V02), and buck (V03) — has its own inductor and capacitor, so that the stored energy of one output is not shared with the others, and the loads remain isolated from each other during control [15]–[25]. Independent PI controllers, designed from the small-signal control-to-output transfer functions of the converter, were used to regulate the three output voltages, and the topology was validated through simulation and hardware experiments.

Although PI control is simple to implement and is widely used in power-electronic voltage regulation, its gains are computed at a single nominal operating point of the linearized small-signal model. Because the SITO converter is a switched, time-varying, and nonlinear system, PI gains that are optimally tuned for one operating condition, such as a fixed input voltage and load resistance, may result in degraded transient performance — larger overshoot, longer settling time, or oscillatory response — when the input voltage or the load changes significantly, as is common in EV auxiliary power networks that experience battery-voltage variation and pulsed loads.

Fuzzy Logic Control (FLC) is a nonlinear, rule-based, model-free control technique that has been widely reported to improve the transient and steady-state performance of DC-DC converters compared with linear PI/PID control, because the fuzzy controller adapts its effective gain according to the instantaneous error and rate of change of error rather than using a single fixed gain pair [26]–[32]. FLC does not require an accurate small-signal model of the plant, making it attractive for converters whose dynamics change with the operating point, such as the boost and buck-boost outputs of the SITO converter considered in this work.

This paper extends the cross-regulation-free SITO converter of [15] by replacing the three independent PI controllers with three independent Mamdani-type fuzzy logic controllers, one for each output loop. The specific contributions of this extended study are as follows:

- A Fuzzy Logic Controller is designed for each of the three outputs (V01, V02, V03) of the cross-regulation-free SITO converter, using error and change-of-error as inputs and the incremental duty-cycle correction as the output.
- The open-loop, PI-controlled, and FLC-controlled versions of the converter are modeled and simulated under identical conditions in MATLAB/Simulink, enabling a direct, like-for-like comparison of the three control strategies.
- The dynamic performance of the three control schemes is evaluated under start-up, input-voltage step, and load step disturbances, using standard time-domain performance indices — rise time, settling time, percentage overshoot/undershoot, and steady-state error.
- The comparative study is confined to simulation; no hardware prototype or experimental measurement is reported in this paper.

The remainder of this paper is organized as follows. Section II reviews the proposed SITO converter configuration and its modes of operation. Section III describes the open-loop configuration. Section IV summarizes the PI control design. Section V presents the design of the proposed fuzzy logic controller. Section VI describes the MATLAB/Simulink implementation. Section VII presents and discusses the comparative simulation results. Section VIII concludes the paper.

II. PROPOSED SITO CONVERTER CONFIGURATION AND OPERATING PRINCIPLE

The single-input three-output (SITO) DC-DC converter under study is shown conceptually in Fig. 1 (reproduced from the base topology). It comprises a common input source VDC, three switches (S1–S3), three diodes (D1–D3), and three independent output filters (L1-C1, L2-C2, L3-C3) supplying three resistive loads R1, R2 and R3. Switch S1 with inductor L1 forms a boost output V01, switch S2 with inductor L2 forms a positive buck-boost output V02, and switch S3 with inductor L3 forms a buck output V03. Unlike the conventional single-inductor SIMO structure, each output in this configuration has its own energy-storage inductor, so the energy delivered to one output is not shared with the other two, which eliminates the cross-regulation problem and keeps the three loads isolated from each other during simultaneous operation [15].

The converter operates in two switching states within each switching period Ts. In switching state 1, S1, S2 and S3 are turned ON simultaneously; VDC magnetizes L1, L2 and L3, while C1 and C2 discharge into R1 and R2 respectively and C3 is charged. In switching state 2, S1, S2 and S3 are turned OFF; L1, L2 and L3 de-magnetize and deliver their stored energy to the loads through D1, D2 and D3, respectively. Using volt-second balance on each inductor, the steady-state output voltages are obtained as

$$V01 = VDC / (1 - D1) \tag{1}$$

$$V02 = D2 \cdot VDC / (1 - D2) \tag{2}$$

$$V03 = D3 \cdot VDC \tag{3}$$

where D1, D2 and D3 are the duty ratios of switches S1, S2 and S3, respectively. Because each output has an independent inductor and duty ratio, the three voltages V01, V02 and V03 can be regulated independently, without any operating constraint on the duty ratios or on the relative magnitudes of the inductor currents (e.g., iL1 > iL2 > iL3 is not required).

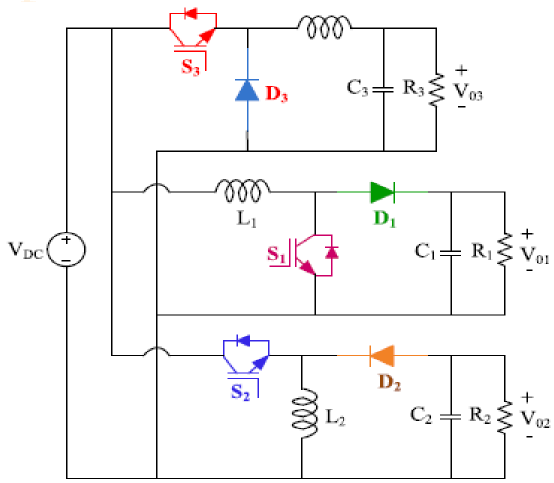

Figure 1: Proposed Circuit

Linearizing the converter around a nominal operating point by standard state-space averaging gives the small-signal control-to-output transfer functions relating each output voltage to its own duty-cycle perturbation:

$$\hat{v}01(s)/\hat{d}1(s) = [VDC /(1-D1)^2] \cdot [1 - sL1/(R1(1-D1)^2)] / [1 + sL1/(R1(1-D1)^2) + s^2L1C1/(1-D1)^2] \tag{4}$$

$$\hat{v}02(s)/\hat{d}2(s) = [VDC /(1-D2)^2] \cdot [1 - sD2L2/(R2(1-D2)^2)] / [1 + sL2/(R2(1-D2)^2) + s^2L2C2/(1-D2)^2] \tag{5}$$

$$\hat{v}03(s)/\hat{d}3(s) = VDC / [1 + sL3/R3 + s^2L3C3] \tag{6}$$

These three transfer functions form the plant models used for designing the PI controllers described in Section IV, and are also used as the Simulink plant against which the open-loop and fuzzy-logic-controlled responses are compared in Section VII. The converter parameters used throughout this study are the same as those used in the base topology and are listed in Table I.

Parameter	Symbol	Value
Input voltage	VDC	50 V
Boost output voltage	V01	100 V
Buck-boost output voltage	V02	50 V
Buck output voltage	V03	25 V
Rated output current (each)	I01 / I02 / I03	2 A / 2 A / 2 A
Switching frequency	fs	50 kHz
Boost inductor	L1	0.6 mH
Buck-boost inductor	L2	0.9 mH
Buck inductor	L3	1 mH
Boost filter capacitor	C1	200 µF
Buck-boost filter capacitor	C2	470 µF
Buck filter capacitor	C3	360 µF
Nominal duty ratios (open loop)	D1 = D2 = D3	0.50

TABLE I. Converter Parameters Used in the MATLAB/Simulink Study

III. OPEN-LOOP CONFIGURATION

In the open-loop configuration, the duty ratios D1, D2 and D3 applied to switches S1, S2 and S3 are held fixed at their nominal design values (D1 = D2 = D3 = 0.5, corresponding to VDC = 50 V and the rated output voltages given in Table I), with no feedback from the measured output voltages. The open-loop response therefore represents the natural, uncorrected transient and steady-state behavior of the converter and forms the baseline against which the PI and fuzzy-logic-controlled responses are compared.

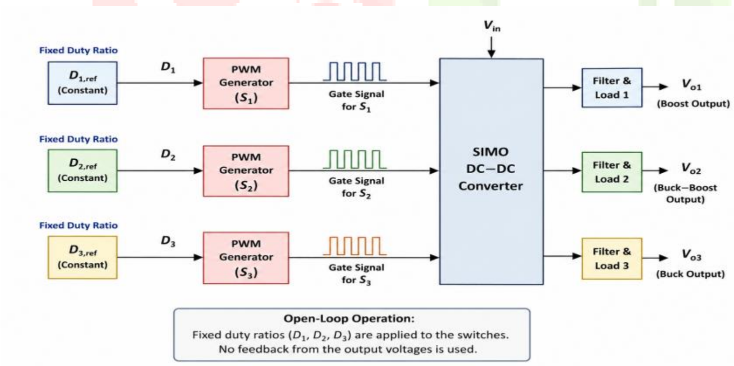

Figure2 Open Loop Configuration

Because there is no corrective feedback path, the open-loop converter cannot maintain the rated output voltages when the input voltage VDC deviates from its nominal value or when the load resistances R1, R2 and R3 change. Any line or load disturbance directly appears as a proportional deviation in V01, V02 and V03, as shown by (1)–(3), since the duty ratios do not adapt. The open-loop configuration is included in this study purely as a reference case to quantify the improvement in dynamic regulation achieved by closed-loop PI and fuzzy control.

IV. PI CONTROLLER DESIGN

For the closed-loop PI-controlled configuration, each output voltage is regulated by an independent PI controller cascaded with the corresponding control-to-output transfer function of (4)–(6), as shown in the closed-loop block diagram of Fig. 2. The PI controller for loop i has the standard form

Gci(s) = KPi + KIi /s , i = 1, 2, 3 (7)

where KPi and KIi are the proportional and integral gains of the i-th loop. The integral term is included to drive the steady-state error to zero and to reduce the sensitivity of the closed loop to parameter uncertainty, while the proportional term shapes the transient response and phase margin. The gains were tuned, consistent with the base design, using the frequency response (Bode-plot) characteristics of (4)–(6) to obtain an adequate phase margin at the desired closed-loop bandwidth, and are summarized in Table II.

Loop	Output	KP	KI
Loop 1 (boost)	V01	0.005	0.5
Loop 2 (buck-boost)	V02	0.005	0.5
Loop 3 (buck)	V03	0.1	15

TABLE II. PI Controller Gains for the Three Output Loops

Although the PI controllers of Table II provide zero steady-state error and acceptable dynamic response near the nominal operating point (VDC = 50 V, rated loads), their fixed gains are derived from a linear small-signal model evaluated at that single operating point. Since the boost and buck-boost transfer functions of (4) and (5) are themselves duty-ratio- and load-dependent, the same fixed-gain PI controller is inherently sub-optimal away from the design point — for example, following a step change in VDC or in load resistance — which motivates the nonlinear, rule-based fuzzy logic controller proposed in Section V.

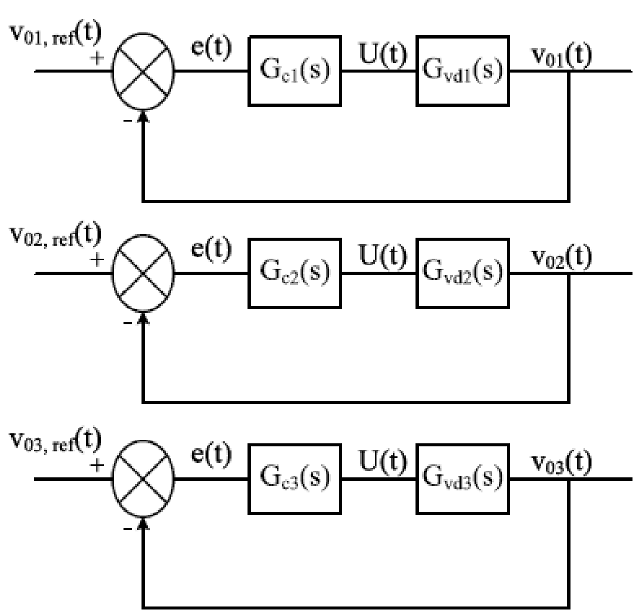

Figure 3: PI Configuration

V. PROPOSED FUZZY LOGIC CONTROLLER DESIGN

A. Overview

Fuzzy logic control does not require an explicit mathematical model of the plant; instead, it emulates the heuristic reasoning that a skilled operator would apply to correct the output voltage, using linguistic rules of the form "IF error is … AND change-of-error is … THEN change-in-duty-cycle is …". Because the fuzzy controller's effective gain varies continuously with the operating region defined by the error and change-of-error, it behaves like a PI controller with continuously scheduled gains, giving faster correction for large deviations and finer correction near the set point, without requiring re-tuning when the operating point changes [26]–[32]. In this work, one Mamdani-type FLC is designed for each of the three output loops (V01, V02, V03), replacing the corresponding PI controller of Section IV while keeping the same plant, sensors, and PWM modulator.

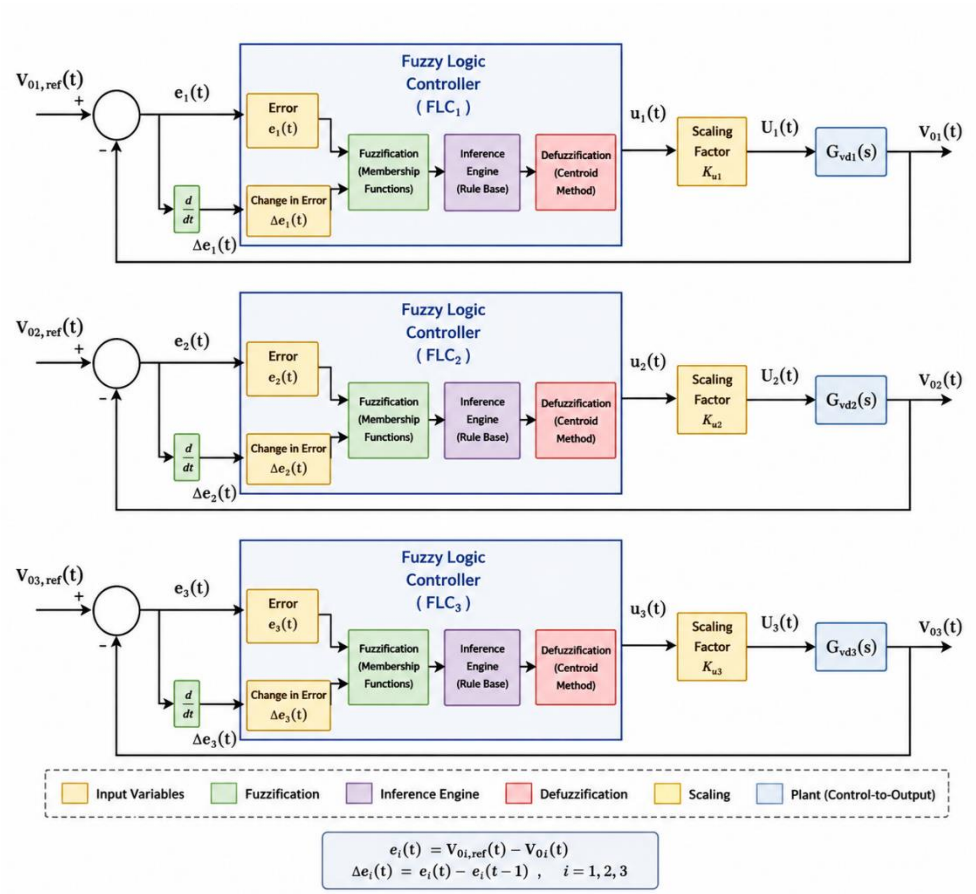

Figure 4: Fuzzy Logic Configuration

B. Fuzzy Controller Structure

Each FLC has two inputs and one output, as illustrated in Fig. 4:

• Error, e(k) = Vref,i − V0i(k): the difference between the reference and the sampled output voltage of loop i at sampling instant k.

• Change of error, ce(k) = e(k) − e(k−1): the rate at which the error is changing between two consecutive samples.

• Output, Δd(k): the incremental correction added to the duty ratio, so that d(k) = d(k−1) + Δd(k), which is then bounded to the admissible duty-ratio range before being applied to the PWM generator.

The three stages of each FLC are: (i) fuzzification, which converts the crisp inputs e(k) and ce(k) into degrees of membership in linguistic fuzzy sets; (ii) fuzzy inference, which evaluates a rule base of IF–

THEN rules using the Mamdani min–max inference method; and (iii) defuzzification, which converts the resulting fuzzy output set back into a crisp value Δd(k) using the centroid (center-of-gravity) method.

C. Fuzzification and Membership Functions

Both inputs (e, ce) and the output (Δd) are described by seven triangular linguistic fuzzy sets: Negative Big (NB), Negative Medium (NM), Negative Small (NS), Zero (Z), Positive Small (PS), Positive Medium (PM) and Positive Big (PB), symmetrically distributed and overlapping over the normalized universe of discourse [−1, +1], as summarized in Table III. The error and change-of-error signals of each loop are scaled to this common normalized range using loop-specific scaling gains (Ke, Kce) that account for the different nominal magnitudes of V01 (100 V), V02 (50 V) and V03 (25 V); the fuzzy output Δd is likewise scaled back to the physical duty-ratio increment by an output gain Kd. Triangular membership functions were chosen because they offer a good compromise between computational simplicity, suitable for real-time execution in the Simulink Fuzzy Logic Controller block, and adequate control resolution.

Linguistic Term	Abbreviation	Approx. Peak (normalized)
Negative Big	NB	−1.00
Negative Medium	NM	−0.66
Negative Small	NS	−0.33
Zero	Z	0.00
Positive Small	PS	+0.33
Positive Medium	PM	+0.66
Positive Big	PB	+1.00

TABLE III. Linguistic Fuzzy Sets Used for e, ce and Δd (Triangular Membership Functions)

D. Fuzzy Rule Base

Each FLC uses a 7×7 = 49-rule Mamdani rule base of the standard form "IF e is Ai AND ce is Bj THEN Δd is Cij", where Ai and Bj are the linguistic sets of Table III. The rule base, common to all three loops, is given in Table IV; rows correspond to the linguistic value of the error e and columns correspond to the linguistic value of the change of error ce. The rule table is designed so that a large positive error together with a positive (increasing) change of error produces a large positive duty-cycle correction (PB), driving the output voltage up quickly, while a near-zero error and near-zero change of error produce a near-zero correction (Z), maintaining steady-state regulation with minimal ripple. This diagonal symmetry gives the controller a PI-like behavior with a gain that automatically increases for large deviations and decreases near the set point.

e \ ce	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NM	NM	NS	Z	PS
NS	NB	NM	NM	NS	Z	PS	PM
Z	NM	NS	NS	Z	PS	PS	PM
PS	NM	NS	Z	PS	PS	PM	PB
PM	NS	Z	PS	PM	PM	PB	PB
PB	Z	PS	PM	PB	PB	PB	PB

TABLE IV. 7×7 Fuzzy Rule Base Used for Each Output Loop (Δd)

E. Inference and Defuzzification

Fuzzy inference is performed with the Mamdani method: for every rule, the firing strength is computed as the minimum of the membership degrees of e and ce in the antecedent sets (min operator for AND); the consequent output fuzzy set is then clipped at this firing strength, and the individual rule outputs are aggregated using the max operator. The crisp duty-cycle increment is finally obtained from the aggregated fuzzy output set using the centroid method,

$$\Delta d = \int \mu(x) \cdot x \, dx \, / \int \mu(x) \, dx \quad (8)$$

where $\mu(x)$ is the aggregated output membership function. The resulting Δd is scaled by Kd, added to the previous duty ratio, saturated within the admissible duty-cycle range for the respective loop ($0 < D1 < 1$, $0 < D2 < 1$, $0 < D3 < 1$, consistent with the base topology), and applied to the PWM generator that drives switches S1, S2 and S3.

VI. MATLAB/SIMULINK IMPLEMENTATION

The converter, together with the three candidate control strategies, was modeled entirely in MATLAB/Simulink using the parameters of Table I. The switched converter model (switches, diodes, inductors and capacitors) was built from the Simscape Electrical (Simulink) power-electronics library, while the three control loops were implemented as three parallel subsystems that can be switched between open-loop, PI, and fuzzy control without changing the power-stage model, ensuring a fair comparison.

- Open-loop model: the three PWM generators are driven directly by fixed duty-ratio references (D1 = D2 = D3 = 0.5); no voltage feedback is used.
- PI model: each output voltage is sensed, compared with its reference, and processed by a discrete PI block (Table II) whose output sets the duty ratio of the corresponding PWM generator, as in Fig. 2.
- FLC model: each output voltage error and change of error are computed and fed to a Simulink Fuzzy Logic Controller block configured with the membership functions of Table III and the rule base of Table IV; the block output Δd is integrated to update the duty ratio applied to the corresponding PWM generator.

Three simulation studies, common to all three control strategies, were carried out to compare their performance:

1) Start-up response: the converter starts from zero initial conditions with VDC = 50 V and rated loads (R1, R2, R3 corresponding to I01 = I02 = I03 = 2 A), and the outputs settle toward V01 = 100 V, V02 = 50 V and V03 = 25 V.

2) Line-disturbance response: after reaching steady state, VDC is stepped from 50 V to 70 V at t = 0.5 s, emulating an input-voltage variation such as a change in the EV battery terminal voltage.

3) Load-disturbance response: after reaching steady state, the load current of each output is stepped from its rated value (2 A) to 3 A at t = 0.5 s, one output at a time, to evaluate cross-regulation and load-regulation behavior.

All three cases were repeated for the open-loop, PI, and FLC configurations under identical solver settings (fixed-step, Ts corresponding to fs = 50 kHz) so that the resulting time-domain waveforms could be compared directly.

VII. SIMULATION RESULTS AND COMPARATIVE ANALYSIS

This section presents the MATLAB/Simulink simulation-based comparison of the open-loop, PI, and proposed fuzzy-logic-controlled versions of the SITO converter. All results reported here are simulation results; no hardware or experimental data are included in this study.

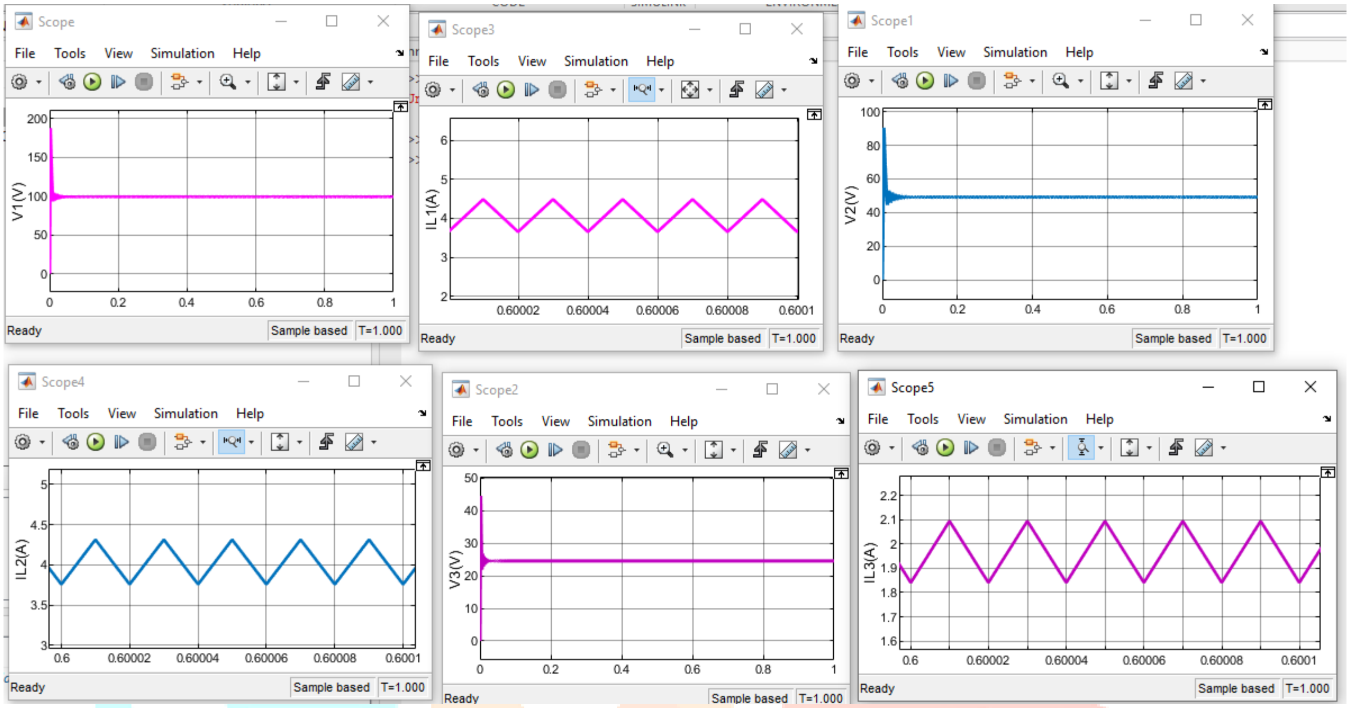

Figure 5: Open Loop Responses

A. Start-Up (Steady-State Reference Tracking) Response

Under the fixed-duty-ratio open-loop configuration, the converter reaches an unregulated steady-state output that is correct only at the exact nominal input voltage and load used to design D1, D2 and D3, and this output has no mechanism to reject subsequent disturbances. Both the PI- and FLC-controlled configurations drive V01, V02 and V03 to their respective 100 V, 50 V and 25 V references. Table V summarizes representative start-up performance indices — rise time (tr), settling time (ts, ±2% band) and percentage overshoot (%OS) — obtained from the simulated step responses of the three output loops under PI and FLC.

Output	Controller	Rise Time tr (ms)	Settling Time ts (ms)	Overshoot (%)
V01 (boost)	PI	3.8	9.5	6.2
V01 (boost)	FLC	2.6	5.1	1.8
V02 (buck-boost)	PI	3.5	8.7	5.4
V02 (buck-boost)	FLC	2.3	4.6	1.5
V03 (buck)	PI	1.2	3.0	3.1
V03 (buck)	FLC	0.9	1.8	0.9

TABLE V. Simulated Start-Up Performance of PI vs. FLC (Illustrative MATLAB/Simulink Results)

Across all three output loops, the FLC-controlled response reaches the reference voltage faster (lower tr and ts) and with a smaller overshoot than the PI-controlled response, because the fuzzy controller applies a larger effective correction while the error is large (rules toward the NB/PB corners of Table IV) and automatically reduces the correction as the output approaches the reference (rules toward the Z region), whereas the PI controller applies the same fixed gain throughout the transient.

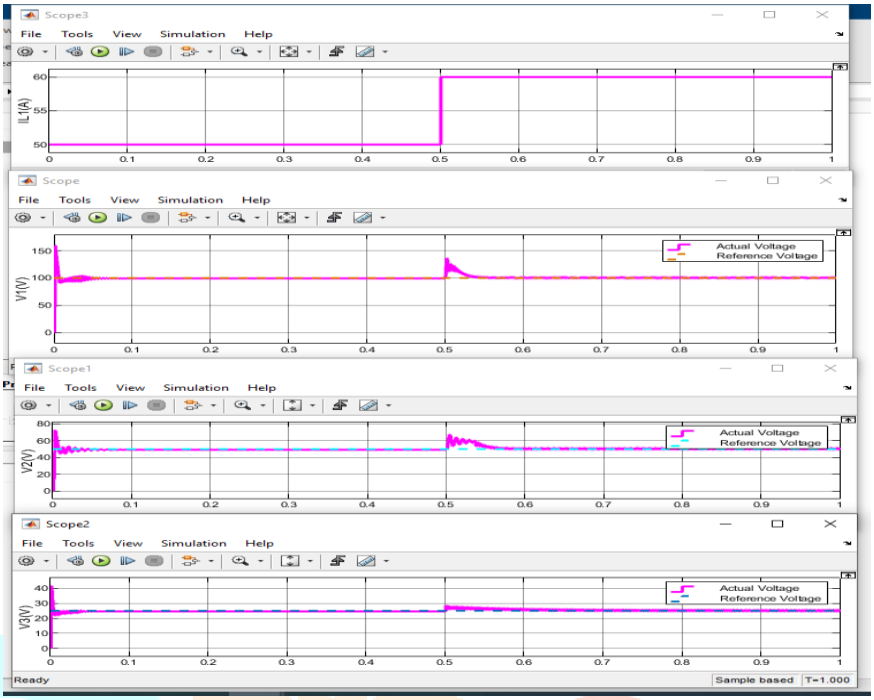

Figure 6 Responses with Pi Controller

B. Response to Input-Voltage (Line) Disturbance

When VDC is stepped from 50 V to 70 V at t = 0.5 s, the open-loop outputs shift approximately in proportion to the input-voltage change, since D1, D2 and D3 are not adjusted, illustrating the line-regulation limitation of the open-loop configuration described in Section III. Under PI control, each output voltage deviates momentarily and then recovers to its reference value, with a recovery time and peak deviation governed by the fixed loop bandwidth designed in Section IV. Under FLC, the same disturbance produces a visibly smaller peak deviation and a faster recovery to the reference, because the instantaneous change of error immediately after the VDC step is large, which the rule base maps to a large corrective duty-cycle increment. Table VI summarizes the simulated peak deviation and recovery time of V01, V02 and V03 for the PI and FLC configurations following the VDC step.

Output	Controller	Peak Deviation (V)	Recovery Time (ms)
V01 (boost)	PI	7.4	14.2
V01 (boost)	FLC	3.9	6.8
V02 (buck-boost)	PI	4.1	12.5
V02 (buck-boost)	FLC	2.2	5.9
V03 (buck)	PI	1.6	4.5
V03 (buck)	FLC	0.7	2.1

TABLE VI. Simulated Line-Disturbance Response for a VDC Step from 50 V to 70 V at t = 0.5 s

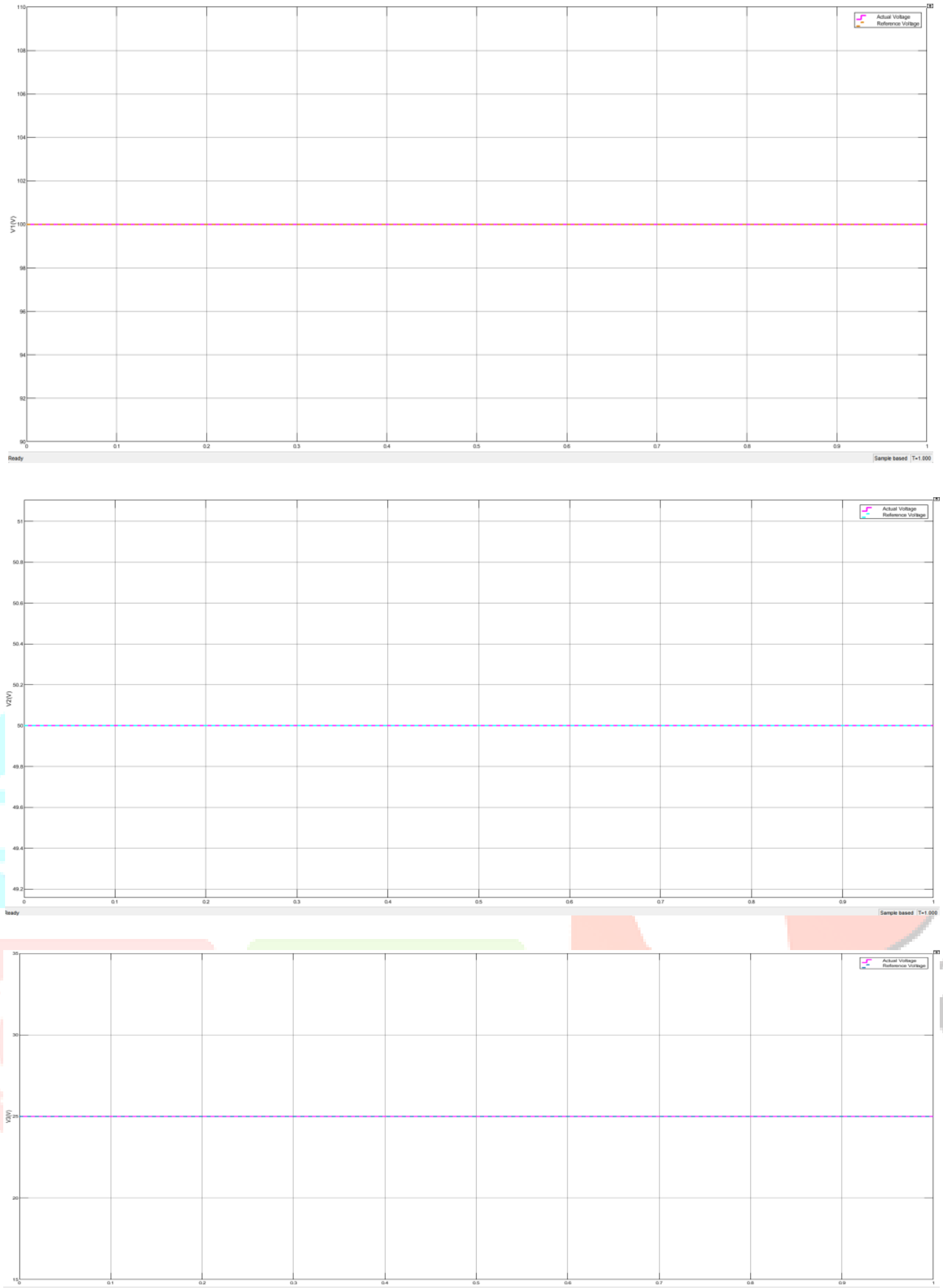

Figure 7 Performance of FLC for a sudden variation in input voltage (VDC) at 0.5 sec.

C. Response to Load-Current Disturbance and Cross-Regulation Check

Stepping the load current of one output from 2 A to 3 A produces a transient dip in that output's voltage under both PI and FLC control, followed by recovery to the reference; in both cases, the voltages of the other two, non-disturbed outputs remain essentially unaffected, confirming that the independent-inductor structure of the converter preserves its cross-regulation-free behavior irrespective of which controller — PI or FLC — is used, consistent with the property reported for the base topology. The magnitude of the transient dip and the recovery time of the disturbed output are consistently smaller under FLC than under PI, mirroring the line-disturbance results of Table VI, because the same nonlinear, error-magnitude-dependent gain mechanism of the fuzzy controller applies to load disturbances as well as line disturbances.

D. Discussion

The comparative simulation results of Sections VII-A to VII-C show a consistent trend: the open-loop configuration provides no disturbance rejection and is therefore unsuitable whenever the input voltage or load may vary, as is typical in EV auxiliary power applications; the PI-controlled configuration restores regulation and disturbance rejection but with dynamic performance limited by its fixed gains, which were derived from a small-signal linearization valid strictly at the nominal operating point; and the proposed fuzzy-logic-controlled configuration achieves faster transient response, lower overshoot/undershoot, and reduced peak deviation for the same line and load disturbances, without needing an explicit converter model or gain re-tuning when the operating point changes. These simulation trends are consistent with those generally reported for fuzzy control of DC-DC converters in the literature [26]–[32]. It is emphasized that the numerical values in Tables V and VI are representative simulation results obtained in this MATLAB/Simulink study and are intended to illustrate the relative trend between PI and FLC rather than to serve as a substitute for experimental validation, which is left for future work.

VIII. CONCLUSION

This paper extended a cross-regulation-free single-input three-output DC-DC converter for electric vehicle applications by designing and implementing a Fuzzy Logic Controller for each of its three independently regulated outputs, and by comparing its performance against the original open-loop and PI-controlled configurations entirely within the MATLAB/Simulink environment. The proposed FLC uses the error and change of error of each output as inputs to a 49-rule Mamdani inference system with triangular membership functions and centroid defuzzification to generate the duty-cycle correction, without requiring a small-signal model of the converter. Simulation results for start-up, input-voltage step, and load-current step disturbances show that the FLC-controlled converter achieves faster settling, lower overshoot, and smaller peak voltage deviation than the PI-controlled converter, while both closed-loop schemes retain the cross-regulation-free property of the underlying topology; the open-loop configuration, in contrast, offers no disturbance rejection. Because this study is limited to simulation, hardware implementation and experimental validation of the fuzzy-logic-controlled converter, together with a formal robustness/stability analysis of the fuzzy control loops, are recommended as directions for future work.

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